A6 a Gilbert multiplier cell. See, for example, Analog Integrated Circuits for Communication, Principles, Simulation and Design, Donald O. Pederson and Kartikeya Mayaram, Kluwer Academic Publishers, Third Printing, 1994, pp. 431-433.

CONT

**In the Claims**

Cancel claims 1-252 and add new claims 253-284 as follows.

253. CMOS transmitter carrier circuitry configured to receive a digital clock signal, the circuitry comprising:

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a phase locked loop including a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple and control circuitry to maintain a desired frequency, the phase locked loop having an output providing a transmitter carrier; and

divider circuitry having an input coupled to the voltage controlled oscillator and receiving the multiplied frequency, the divider circuitry being configured to divide by the predetermined multiple, and the divider circuitry having an output coupled to the control circuitry.

254. CMOS transmitter carrier circuitry in accordance with claim 253, wherein:

the phase locked loop includes a loop filter coupled to the voltage controlled oscillator, and the control circuitry comprises:

a phase-frequency detector coupled to the divider circuitry output ; and

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a charge pump, the phase-frequency detector and the charge pump being coupled to the voltage controlled oscillator and to the loop filter, wherein the loop filter is a passive loop filter.

255. CMOS transmitter carrier circuitry in accordance with claim 253, wherein the voltage controlled oscillator has a plurality of outputs that are configured to be angularly spaced apart with respect to phase.

256. CMOS transmitter carrier circuitry in accordance with claim 255, further comprising a frequency doubler that receives at least some of the angularly spaced apart outputs of the voltage controlled oscillator, and that is configured to produce a signal with a frequency that is double the frequency of the outputs of the voltage controlled oscillator.

CONT

257. CMOS transmitter carrier circuitry in accordance with claim 256, wherein the frequency doubler comprises first and second Gilbert cells coupled together, a frequency generator configured to apply a first sinusoidal wave to the first Gilbert cell, and a phase shifter coupled between the first and second Gilbert cells to apply to the second Gilbert cell a sinusoidal wave that is shifted from the first sinusoidal wave.

258. CMOS transmitter carrier circuitry in accordance with claim 253, wherein the charge pump comprises:

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a first charge pump coupled to a start-up circuit and configured to pump a frequency of the voltage controlled oscillator up in coarse, medium or medium fine steps in response to a start-up command from the start-up circuit; and

a second charge pump coupled to the control circuitry and configured to pump up or down the frequency of the voltage controlled oscillator in fine steps in response to signals from the control circuitry.

CONT

259. CMOS transmitter carrier circuitry in accordance with claim 258, wherein the start-up circuit is configured to initially invoke coarse or medium steps to pump up the frequency of the voltage controlled oscillator and is configured to invoke medium fine or fine steps when the start-up circuit determines that the frequency of the voltage controlled oscillator is within a few percent of a desired frequency.

260. A CMOS transmitter configured to receive a digital clock signal, the transmitter comprising:

a phase locked loop including a voltage controlled oscillator multiplying the frequency of the digital clock signal by a predetermined multiple, control circuitry coupled to the phase locked loop to maintain a desired frequency, the voltage controlled oscillator having a plurality of outputs that are angularly spaced apart with respect to phase, the phase locked loop having an output providing a transmitter carrier;

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divider circuitry having an input coupled to at least one of the outputs of the voltage controlled oscillator, the divider circuitry being configured to divide by the predetermined multiple and having an output coupled to the control circuitry; and

a modulator coupled to the phase locked loop to use the transmitter carrier.

261. A CMOS transmitter in accordance with claim 260, wherein the voltage controlled oscillator has outputs that are spaced apart, with respect to phase in 45 degree intervals.

CONT

262. A CMOS transmitter in accordance with claim 261, wherein the predetermined multiple is sixteen.

263. A CMOS transmitter in accordance with claim 260, wherein the control circuitry comprises:

a passive loop filter;

a phase-frequency detector, the divider circuitry output being coupled to the phase-frequency detector; and

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a charge pump coupled to the voltage controlled oscillator and to the loop filter.

264. A CMOS transmitter in accordance with claim 263, wherein the charge pump comprises:

a first charge pump coupled to a start-up circuit and configured to pump a frequency of the voltage controlled oscillator up in coarse, medium or medium fine steps in response to a start-up command from the start-up circuit; and

a second charge pump coupled to the control circuitry and configured to pump up or down the frequency of the voltage controlled oscillator in fine steps in response to signals from the phase-frequency detector.

CONT

265. A CMOS transmitter in accordance with claim 264, wherein the start-up circuit is configured to initially invoke coarse or medium steps to pump up the frequency of the voltage controlled oscillator and is configured to invoke medium fine or fine steps when the start-up circuit determines that the frequency of the voltage controlled oscillator is within a few percent of a desired frequency.

266. An integrated circuit including carrier circuitry configured to provide a carrier for wireless communications, the carrier circuitry being configured to receive a digital clock signal, the carrier circuitry being defined by CMOS circuit elements, the carrier circuitry comprising:

a phase locked loop including a voltage controlled oscillator multiplying the frequency of the digital clock signal by a predetermined multiple, control circuitry configured compare the frequency and phase of the digital clock signal to a second signal and to issue pump up or pump down signals in response to the comparison, and a charge pump coupled to the control circuitry and configured to maintain a desired frequency in response to the pump up and pump down signals, the charge pump being configured to receive the pump up and pump down signals and produce an output having a voltage that varies in response to the pump up and pump down signals, the voltage controlled oscillator having an output, the phase locked loop having an output providing a transmitter carrier; and

divider circuitry having an input coupled to the output of the voltage controlled oscillator, the divider circuitry being configured to divide by the predetermined multiple and having an output coupled to the control circuitry.

267. An integrated circuit in accordance with claim 266, wherein the divider circuitry output defines the second signal and the control circuitry comprises a loop filter, a phase-frequency detector receiving the digital clock signal and the second signal and performing the comparison, the frequency of the output of the voltage controlled oscillator being configured to vary depending on a voltage provided by the loop filter to the voltage controlled oscillator.

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CONT

268. An integrated circuit in accordance with claim 267 wherein the loop filter is configured to filter the output of the charge pump.

269. An integrated circuit in accordance with claim 266 wherein the predetermined multiple is sixteen.

270. An integrated circuit in accordance with claim 266, wherein the charge pump comprises:

a first charge pump coupled to a start-up circuit and configured to pump a frequency of the voltage controlled oscillator up in coarse, medium or medium fine steps in response to a start-up command from the start-up circuit; and

a second charge pump coupled to the control circuitry and configured to pump up or down the frequency of the voltage controlled oscillator in fine steps in response to signals from the phase-frequency detector.

271. An integrated circuit in accordance with claim 270, wherein the start-up circuit is configured to initially invoke coarse or medium steps to pump up the frequency of the voltage controlled oscillator and is configured to invoke medium fine or fine steps when the start-up circuit determines that the frequency of the voltage controlled oscillator is within a few percent of a desired frequency.

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CONT

272. An integrated circuit including carrier circuitry configured to provide a carrier signal for wireless communications, the carrier circuitry being configured to receive a digital clock signal, the carrier circuitry being defined by CMOS circuit elements and comprising:

a phase locked loop including a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple, control circuitry configured to receive the digital clock signal and compare the frequency and phase of the digital clock signal with a second signal and configured to issue pump up or pump down signals in response to the comparison, and a charge pump coupled to the control circuitry and to the voltage controlled oscillator to maintain a desired frequency in response to the pump up and pump down signals, the voltage controlled oscillator having a plurality of outputs that are angularly spaced apart with respect to phase, the phase locked loop having an output providing a transmitter carrier; and

divider circuitry having an input coupled to at least one of the outputs of the voltage controlled oscillator, the divider circuitry dividing by the predetermined multiple and having an output defining the second signal coupled to the control circuitry.

273. An integrated circuit in accordance with claim 272 wherein the predetermined multiple is sixteen.

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274. An integrated circuit in accordance with claim 272 wherein the control circuitry comprises:

a passive loop filter coupled to the phase locked loop; and

a phase-frequency detector coupled to the charge pump;

CONT

and further comprising a first frequency doubler configured to receive at least some of the angularly spaced apart outputs of the voltage controlled oscillator, and that is configured to produce a signal with a frequency that is double the frequency of the outputs of the voltage controlled oscillator.

275. An integrated circuit in accordance with claim 274 and further comprising a second frequency doubler coupled to the first frequency doubler and that is configured to produce a signal with a frequency that is double the frequency of the signal produced by the first frequency doubler.

276. An integrated circuit in accordance with claim 272 and further comprising a first frequency doubler stage including a first frequency doubler configured to receive at least some of the angularly spaced apart outputs of the voltage controlled oscillator, and that is configured to produce a signal with a frequency that is double the frequency of the outputs of the voltage controlled oscillator, and a second frequency doubler that receives other of the angularly spaced apart outputs of the voltage controlled oscillator, and that is configured to produce a signal with a frequency that is double the frequency of the outputs of the voltage controlled oscillator.

277. An integrated circuit in accordance with claim 276 and further comprising a second frequency doubler stage coupled to the first frequency doubler stage and that is configured to produce a signal with a frequency that is double the frequency of the signals produced by the first frequency doubler stage.

278. An integrated circuit in accordance with claim 272, wherein the charge pump comprises:

a first charge pump coupled to a start-up circuit and configured to pump a frequency of the voltage controlled oscillator up in coarse, medium or medium fine steps in response to a start-up command from the start-up circuit; and

a second charge pump coupled to the control circuitry and configured to pump up or down the frequency of the voltage controlled oscillator in fine steps in response to signals from the phase-frequency detector.

279. An integrated circuit in accordance with claim 278, wherein the start-up circuit is configured to initially invoke coarse or medium steps to pump up the frequency of the voltage controlled oscillator and is configured to invoke medium fine or fine steps when the start-up circuit determines that the frequency of the voltage controlled oscillator is within a few percent of a desired frequency.

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CONT

280. A communications system including a transmitter integrated circuit for wireless communications, the transmitter integrated circuit being configured to receive a digital clock signal, the transmitter integrated circuit being defined by CMOS circuit elements and comprising:

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a phase locked loop including a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple, control circuitry configured to receive the digital clock signal and to compare the frequency and phase of the digital clock signal with a second signal and to issue pump up or pump down signals in response to the comparison, and a charge pump coupled to the control circuitry and the voltage controlled oscillator to maintain a desired frequency in response to the pump up and pump down signals, the voltage controlled oscillator having a plurality of outputs that are angularly spaced apart with respect to phase, the phase locked loop having an output providing a transmitter carrier;

CONT

divider circuitry having an input coupled to at least at least one of the outputs of the voltage controlled oscillator, the divider circuitry dividing by the predetermined multiple and having an output defining the second signal coupled to the control circuitry; and

a modulator coupled to the voltage controlled oscillator.

281. A communications system in accordance with claim 280, wherein the voltage controlled oscillator includes a plurality of stages, one of the stages including a first transistor having a control electrode defining a first input, and first and second power electrodes, wherein the first power electrode defines a first node, wherein the stage further includes a second transistor having a control electrode defining a second input, and having first and second power electrodes, wherein the first power electrode of the second transistor defines a second node, wherein the stage further includes a current source connected to the second power electrodes of the first and second transistors, the current source being configured to direct current away from the second power electrodes of the first and second transistors, and wherein the stage further includes a variable resistance configured to couple the first and second nodes to a supply voltage.

282. A communications system in accordance with claim 280, wherein the control circuitry comprises:

a passive loop filter coupled to the phase locked loop and to the charge pump; and

a phase-frequency detector coupled to the second signal and to the charge pump.

283. A communications system in accordance with claim 280, wherein the charge pump comprises:

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a first charge pump coupled to a start-up circuit and configured to pump a frequency of the voltage controlled oscillator up in coarse, medium or medium fine steps in response to a start-up command from the start-up circuit; and

a second charge pump coupled to the control circuitry and configured to pump up or down the frequency of the voltage controlled oscillator in fine steps in response to signals from the phase-frequency detector.

CONT

284. A communications system in accordance with claim 283, wherein the start-up circuit is configured to initially invoke coarse or medium steps to pump up the frequency of the voltage controlled oscillator and is configured to invoke medium fine or fine steps when the start-up circuit determines that the frequency of the voltage controlled oscillator is within a few percent of a desired frequency.